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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/358,388	07/21/1999	KAORI UMEZAWA	0039-79292-2	1515

22850 7590 07/09/2004

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/358,388	UMEZAWA ET AL.
	Examiner	Art Unit
	Anh D. Mai	2814

-- The MAILING DATE of this communication appears on th cover sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-11,14,15,24-46 and 48-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-11,14,15,24-46 and 48-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed April 29, 2004 has been entered. Claims 16-23 have been canceled. Claims 9, 25-29 and 36 have been amended. Claims 9-11, 14, 15, 24-46 and 48-53 are pending.

Response to Amendment

2. The amendment filed April 29, 2004 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "without using doped silicon oxide containing a melting-temperature-lowering dopant of boron or phosphorous for lowering the melting-temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization"; "which does not contain the melting temperature lowering dopant" and "by annealing the semiconductor substrate so as not to melt the oxide film" (as recited in amended claims 9, 25-29 and 36"

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 9-11, 14, 15, 24-46 and 48-53 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "without using doped silicon oxide containing a melting temperature lowering dopant of boron or phosphorous for lowering the melting temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization"; "which does not contain the melting temperature lowering dopant" and "by annealing the semiconductor substrate so as not to melt the oxide film" in the application as filed.

MPEP 2173.05(i) states: "Any negative limitation or exclusionary proviso **must have** basis in the original disclosure", *In re Schechter*, 205 F2.d 185, 98 USPQ 144 (CCPA 1953).

These subject matters could not find support from the original specification, thus, have been considered as new matters and will be treated as such.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 9-11, 14, 15, 24-29, 34-45 and 48-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. (U.S. Patent No. 4,571,819) (hereinafter Rogers) in view of Lee et al. (U.S. Patent No. 4,952,524) (hereinafter Lee) (all of record).

With respect to claim **9**, as best understood by the examiner, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) depositing oxide films (19) in the grooves by a CVD method;

(c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the active areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(d) after the removing, annealing the semiconductor substrate (10) at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized. (See Figs. 2-8).

Thus, Rogers is shown to teach all of the features of the claim with the exception of explicitly using an electrically inert organic silicon source for the CVD oxide film (19).

However, Lee teaches the electrically inert organic silicon source such as TEOS are well known in the art to be used as silicon source for the oxide film (25).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to deposit the oxide film (19) of Rogers using electrically inert

organic silicon source, TEOS, as taught by Lee because electrically inert organic silicon source, TEOS, is less toxic and easy to handle. This is well known in the art.

Note that changing the ring structure of the oxide film and reducing dislocation density of the substrate are inherent result of the high temperature annealing of the substrate following the filling of the trench with oxide film. Since the annealing temperature of Rogers is within the claimed range, (>1150 °C to <1300 °C), therefore, the dislocation density generated in the corresponding device region in a vicinity of the grooves (13) of Rogers is inherently less than $1/\mu m^2$.

With respect to claim 10, the depositing method of Rogers includes one of the methods as claimed.

With respect to claim 11, the ambient during the anneal of Rogers includes nitrogen gas.

With respect to claim 14, trench (13) of Rogers appears to have a depth (d) to width (l) ratio of less than 10.

With respect to claims 15 and 24, the arrangement of the grooves on the semiconductor substrate is clearly a design choice. The method of forming the STI is disclosed.

With respect to claim **25**, as best understood by the examiner, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) depositing oxide films (19) in the grooves by a CVD method;

(c) annealing the semiconductor substrate (10) at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized; and

(d) removing upper parts of the oxide films, after the annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the active areas of the semiconductor substrate serving as a top surface of a corresponding device region. (See Figs. 2-8).

With respect to using electrically inert organic silicon source, changing ring structure and dislocation density, similar reasoning as that of claim 9 is also applied.

With respect to claims **26** and **27**, as best understood by the examiner, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) burying oxide films (19) in the grooves (13) by a CVD method;

(c) annealing the semiconductor substrate (10) at a substrate temperature of which is greater than or equal to 1150 °C but less than 1350 °C. (See Figs. 2-8).

With respect to using electrically inert organic silicon source and changing ring structure, similar reasoning as that of claim 9 is also applied.

With respect to etching rate by ammonium fluoride solution of the oxide film less than 130 nm/min, it is well known in the art that under a high temperature anneal (≥1150 °C and ≤1350 °C) , the oxide film is densified and the density of the oxide film is approaching that of thermal oxide, hence the etch rate.

With respect to claim **28**, as best understood by the examiner, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) forming a thin thermal oxidation film (16) on the inner wall of the grooves;

(c) depositing oxide films (19) directly on the thin thermal oxidation film by a CVD method;

(d) removing upper parts of the oxide films (19) so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as top surface of a corresponding device region; and

(e) annealing the semiconductor substrate (10), after the removing, at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation

density generated in the corresponding device region in a vicinity of the grooves is minimized. (See Figs. 2-8).

With respect to using electrically inert organic silicon source, changing ring structure and dislocation density, similar reasoning as that of claim 9 is also applied.

With respect to depositing oxide films directly on the thin thermal oxidation films, note that the specification contains no disclosure of either the *critical nature of the claimed "oxide film being directly deposited on the thin thermal oxidation films" of any unexpected results arising therefrom*. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen state of deposition are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Further, Applicants admitted previously that "a substitute thermal oxidation film can be used or that both of these alternative can be omitted under the teaching of the paragraph beginning at line 22 of page 19",

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to deposit the oxide film of Rogers directly or indirectly on the thermal oxidation films to fill the trenches without altering the characteristics of the isolation trench.

With respect to claim 34, the thin thermal oxidation films (16) of Rogers are formed by thermal oxidizing inner walls of the grooves (13).

With respect to claim **29**, as best understood by the examiner, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) forming thin thermal oxidation films (16) on the inner walls of the grooves;

(c) depositing oxide films (19) on the thermal oxidation films (16) in the grooves by a CVD method;

(d) annealing the semiconductor substrate (10) at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized; and

(e) removing upper parts of the oxide films, after the annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the active areas of the semiconductor substrate serving as a top surface of a corresponding device region. (See Figs. 2-8).

With respect to using electrically inert organic silicon source, changing ring structure and dislocation density, similar reasoning as that of claim 9 is also applied.

With respect to claim 35, the thin thermal oxidation films (16) of Rogers are formed by thermal oxidizing inner walls of the grooves (13).

With respect to claim **36**, as best understood by the examiner, Rogers teaches a method for forming a microelectronic structure substantially as claimed including:

(a) forming a photoresist mask layer on a substrate (10) wherein the photoresist mask layer exposed a part (12) of the substrate;

(b) forming a groove (13) in the exposed part of the substrate;

(c) depositing a layer of an insulating film (19) so as to fill the groove (13) and cover the substrate;

(d) annealing the semiconductor substrate (10) at a temperature which is greater than or equal to 1150 °C but less than 1350 °C. (See Figs. 2-8).

Thus, Rogers is shown to teach all of the features of the claim with the exception of explicitly depositing the insulating film using an electrically inert organic silicon source and to cover the mask layer (11).

However, Lee teaches forming groove (51) in the exposed part of semiconductor substrate (11) by forming a mask layer (15) under the photoresist mask (17) on the semiconductor substrate (11) wherein the mask layer (15) exposes a part of the semiconductor substrate (11) to protect the surface of the substrate from the plasma of the etch and depositing a layer (25) of an insulating film using an electrically inert organic silicon source (TEOS) so as to fill the groove (51) and cover the mask layer (15).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the mask layer of Rogers including an mask layer (15) under the photoresist mask (17) as taught by Lee to protect the surface of the substrate from the plasma.

With respect to electrically inert organic silicon source (TEOS), it would have been obvious to one having ordinary skill in the art at the time of the invention was made to deposit the layer (19) of insulating film of Rogers using electrically inert organic silicon source, TEOS, as taught by Lee because electrically inert organic silicon source, TEOS, is less toxic and easy to handle.

With respect to claims 37 and 38, the duration (2-8 hrs) of the annealing of Rogers encompassed the claimed duration.

With respect to claims 39 and 40, the annealing of Rogers is performed in an inert atmosphere (N_2).

With respect to claim 41, the method of Rogers further includes planarizing the insulating film (19) so that the substrate (10) is exposed.

With respect to claim 42, the planarizing of Rogers comprises using CDE method.

With respect to claim 43, the forming the mask layer of Rogers, in view of Lee comprises forming an oxide layer (13) on the substrate.

With respect to claim 44, forming the layer of the insulating film (19) of Rogers comprises forming an oxide layer (16) on inner walls of the groove (13) and depositing the insulating material (19) on the oxide layer (16) to fill the groove.

With respect to claim 45, the depositing of insulating material (19) of Rogers, in view of Lee comprises forming an oxide by CVD using the electrically inert organic silicon source (TEOS).

With respect to claim 48, a taper grooves is also contemplated by Lee. (See Fig. 9).

With respect to claim 49, the depositing of the insulating film (19) of Rogers appears to deposit the insulating film at a thickness larger than a half of the width of the groove.

With respect to claim 50, the forming the mask of Rogers is configured to provide a plurality of grooves (13) at a cross sectional view so as to define a SDG region between a couple of the grooves at the cross sectional view.

With respect to claim 51, Rogers teach all of the features of the claim with the exception of explicitly disclose the width of the SDG between the couple of the grooves (13). The claimed width of 0.3μm between the grooves (13) does not appears to be critical.

Note that the specification contains no disclosure of either the critical nature of the claimed *a width of 0.3μm between the grooves* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the SDG region of Rogers having a width as claimed, since such a modification would have involved a mere change in the size of the SDG regions. A change in size is generally recognized as being within the level of ordinary skill in the art. See *In re Rose, 105 USPQ 237 (CCPA 1955).*

With respect to claim 52, the method of Rogers further includes forming source/drain regions (36/37) in the SDG region sandwiched by the grooves (13).

With respect to claim 53, the grooves of Rogers appears to have an aspect ratio of less than 10.

5. Claims 30-33 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers '819 and Lee '524 as applied to claims 9, 25-27 and 36 above, and further in view of Dash et al. (U.S. Patent No. 5,173,439) of record.

Rogers and Lee teaches depositing oxide film (19) in the grooves (13) by a CVD method.

Thus, Roger and Lee are shown to teach all the features of the claim with the exception of depositing the oxide film directly on walls of the grooves.

However, Dash teaches an oxide film (18) can be deposited directly on the walls of the grooves (14/16) to form isolation regions. The limitation of oxide film are deposited directly on the walls of the grooves does not appears to be critical.

Note that the specification contains no disclosure of either the *critical nature of the claimed "oxide film being directly deposited on the walls of the grooves" of any unexpected results arising therefrom*. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen state of deposition are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to deposit the oxide film (19) of Rogers directly on the walls of the grooves as taught by Dash to fill the grooves with dielectric in self-aligning, without void and good planarity.

Response to Arguments

6. Applicant's arguments filed April 29, 2004 have been fully considered but they are not persuasive.

With respect to the objection:

Applicants argue that since the new matters added to the claims, the objection can not be made.

However, it is determined that claims are part of the disclosure. Thus, any new matters added to the claims are considered as added to the specification. Therefore, the objections made previously or concurrently are proper, thus, maintained.

With respect to new matters:

Applicants state: "the description need not be in ipsis verbis [i.e. "in the same words"] to be sufficient".

Applicants appear to contend that Applicants can exclude any matters in the claims if the specification does not positively disclose them.

However, MPEP 2173.05(i) states: "The mere absence of a positive recitation is not basis for an exclusion. Any claim containing a negative limitation which does not have basis in the original disclosure should be rejected under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement".

In the instant case, the specification as filed is completely silent about doped silicon oxide or melting-temperature lowering dopant or not to melt the oxide film, etc.,. The

specification discloses: "The buried oxide film 71 are **oxide film** which are formed by **any organic silicon based CVD** method, spin-on-glass coating method ..., and then annealed at a temperature of 1100 to 1135 °C". (See page6, lines 5-10). There is no exclusion.

Since oxide is well known in the art to include doped or undoped silicon oxide. All of which are used for isolation. Therefore, the exclusion of the doped silicon oxide must be positively recited in the specification. Also, these matters are not inherent.

Regarding the term "**non doped**", Applicants should point out the portion of the specification which support the oxide film to be **non doped**.

Regarding Fig. 7B, this figure is consistent with etching of oxide, doped or undoped. Neither the figures nor the specification indicated that doped oxide is etch differently.

Regarding Figs. 6A-B of the instant application and Figs. 1, 3 and 4 of the Journal of Non-Crystalline Solids, there is no clear indication that the oxide material of Figs. 6A or B are that of pure fused silica, because Figs. 6A-B are more similar to the Raman Spectrum of doped silica, Figs. 3 and 4 than that of the pure fused silica, Fig. 1. In Fig. 1, a pure fused silica should have a spike at 485 and a peak at 440 cm^{-1}, while Figs. 6A-B only show a peak at ~ 490 without a spike.

With respect to the Rejection Under 35 U.S.C 103(a):

Again, Applicants argue that the oxide of Rogers is doped oxide.

As discussed above, the exclusion of the doped oxide are new matters. Rogers clearly teaches deposit oxide to fill the trenches and anneal the substrate at the temperature as claimed.

With respect to the ring structure, it more probable than not the oxide of Rogers after the high temperature anneal should have the ring structure changed. (See Figs. 3 and 4, Journal of Non-Crystalline Solids, IDS).

Applicants further argue: moreover, the outstanding Action fails to present a reasonable motivation as to why the artisan would have abandoned the main objective of Rogers in terms of the col. 6, lines 26-29, described intent to collapse the voids 21-21 and to reflow the upper surface 26 of the glass to a substantially level topography that requires the presence of boron or phosphorous.

However, there is no need to abandon the teaching of Rogers since Rogers clearly teaches all limitations of the claims with the exception depositing the oxide film using an electrically inert organic silicon source, i.e., TEOS, which is taught by Lee. Again, the exclusion of doped oxide have been determined to be new matters. Thus, further discussion about doped oxide is not needed.

With respect to Dash, Dash teaches that it is obvious to fill the trenches without the intervening oxide liner.

Conclusion

7. Although the same references have been applied, the amendment have added new matters into the specification and altered the scope of the claims.

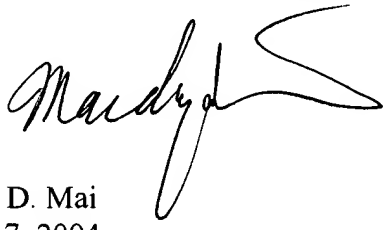
8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Anh D. Mai
July 7, 2004